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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/720,142	12/21/2000	Yoichi Yamada	107300	7514

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/720,142	YAMADA, YOICHI	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10,12-16 and 18-20* is/are rejected.

7)☒ Claim(s) *4,11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to because Figure 13 requires a –Prior Art— tag in order to correspond the material of Figure 13 with that found in the "Background of Art" section of Applicant's Specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Please correct the numbering of the ID generation circuit of page 17, line 10 from "101" to –51--, as seen in Figure 8.

Appropriate correction is required.

Claim Objections

Claims 6, 7 and 14-20 are objected to because of the following informalities:

Regarding claim 6, the claim recites "a register which receives address data of the area where the information is written, from the processor, and stores the address data into the memory". According to Applicant's Specification, the address register (54) stores the address of the memory (53) where the information (ID) is to be stored. The address is passed to the ID Write Circuit (52), which uses the address to write the

information at the address designated by the address register (page 17, lines 9-16). The Examiner is unclear as to how the register "stores the address data into the memory", an operation which is described as the operation done by the ID Write Circuit. The Applicant is encouraged to amend the claim in order to correspond to that which is found in the Specification, such as removing the "stores" limitation. The Examiner will interpret the claim based on Applicant's Specification without the "stores" limitation.

Regarding claim 7, the word –production— needs to be included between "the" and "information" in the third line of the claim in order to facilitate proper antecedent basis according to "production information" as recited in parent claim 1, line 8.

Regarding claim 14, lines 8-9 recite "the external memory through the terminal". The only memory recited in claim 14 is recited as "a memory", without mentioning whether it is external or not. In order to facilitate proper antecedent basis, the word "external" should either be added to "a memory" in line 3 or removed from line 9. Also, changing "the terminal" to "a terminal" would facilitate proper antecedent basis since a terminal had not been previously referenced and claimed. The Examiner will interpret the "external memory" as an internal memory due to Applicant's Specification and Drawings, which only show an IC with a built-in processor also coupled to a built-in memory (Figures 10-12).

Claims 15-20 are objected to as being dependent upon a previously objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 5, and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

Regarding claim 1, AAPA teaches a semiconductor integrated circuit (100) connected to an external processor (200) Figure 13). Built-in memory (103) stores data as a cache memory for the processor (page 1, lines 21-23). Terminal (104) couples the processor to the built-in memory. ID-Generation circuit (101) generates production information (ID) about the semiconductor IC (page 1, lines 23-26). The ID is written into the built-in memory when resetting the IC, where the storing upon resetting constitutes that the operation occurs before normal operation has started (page 2, lines 7-12). Although a write circuit as claimed is not explicitly recited, the AAPA recites "storing the ID" in the built-in memory which inherently requires some command circuitry for writing the ID into the built-in memory.

Regarding claim 2, AAPA teaches that the ID is written into the built-in memory upon an IC system reset, as disclosed above (page 2, lines 7-9).

Regarding claim 5, AAPA teaches that the memory is a cache memory for use by the processor, as disclosed above (page 1, lines 21-23).

Regarding claim 7, AAPA teaches that the production information could include a production history or manufacturer's number (page 1, lines 23-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Ogura (US# 6,181,629).

Regarding claim 3, AAPA teaches storing the ID information when resetting the integrated circuit (page 2, lines 7-9). What AAPA fails to recite is what device causes the (resetting) command to occur. Ogura teaches a semiconductor memory device that includes a (reset) signal under the direction of the CPU (col. 3, lines 61-63). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Ogura at the time the invention was made to modify the processing system of AAPA to include the CPU resetting command/signal of Ogura, because then one circuit (CPU) could be responsible for multiple tasks without wasting space on the I.C. with multiple specialized command circuits and thus reduce the manufacturing costs of the I.C.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Runaldue et al. (US# 6,178,483).

The difference between the claimed subject matter and that of AAPA, disclosed supra, is that the claims recite a register which receives address data related to the location in the memory to which data is to be stored. Runaldue et al. teaches a register for storing an address for a write operation, where the register receives the address from a host and stores an address related to the location in the SDRAM memory were the data is to be written (col. 11, lines 15-21). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Runaldue et al. at the time the invention was made to modify the memory system of AAPA to include the address storing register of Runaldue et al., because then a register, a high-speed memory device, could receive and supply the write address to the system in such a way as to reduce processing time, as taught by Runaldue et al.

Claims 8, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Handy.

Regarding claim 8, AAPA recites a built-in memory found on the integrated circuit and the processor found external to the integrated circuit (Fig. 1). The difference between the claimed subject matter and that of AAPA, disclosed supra, is that the claim recites that the semiconductor IC is connected to a combination of an external memory and processor externally. Handy teaches L1 and L2 caches tied to the processor for

storing data as directed by the processor (page 89, para. 4 – page 90, para. 2). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Handy at the time the invention was made to modify the memory system of AAPA to include the external memory with the processor into the caching system like that of Handy, because then a small high-speed memory could be implemented for quicker data retrieval by the processor as taught by Handy.

Regarding claim 9, AAPA teaches that the ID is written into the built-in memory upon an IC system reset, as disclosed above (page 2, lines 7-9).

Regarding claim 13, AAPA teaches that the production information could include a production history or manufacturer's number (page 1, lines 23-25).

Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Handy, and Ogura (US# 6,181,629).

Regarding claim 10, AAPA teaches storing the ID information when resetting the integrated circuit (page 2, lines 7-9). What AAPA fails to recite is what device causes the (resetting) command to occur. Ogura teaches a semiconductor memory device that includes a (reset) signal under the direction of the CPU (col. 3, lines 61-63). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Handy and Ogura at the time the invention was made to modify the processing system of AAPA and Handy to include the CPU resetting command/signal of Ogura, because then one circuit (CPU) could be responsible for multiple tasks without wasting

space on the I.C. with multiple specialized command circuits and thus reduce the manufacturing costs of the I.C.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Handy, and Runaldue et al. (US# 6,178,483).

The difference between the claimed subject matter and that of AAPA, disclosed supra, is that the claims recite a register which receives address data related to the location in the memory to which data is to be stored. Runaldue et al. teaches a register for storing an address for a write operation, where the register receives the address from a host and stores an address related to the location in the SDRAM memory were the data is to be written (col. 11, lines 15-21). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Handy, and Runaldue et al. at the time the invention was made to modify the memory system of AAPA and Handy to include the address storing register of Runaldue et al., because then a register, a high-speed memory device, could receive and supply the write address to the system in such a way as to reduce processing time, as taught by Runaldue et al.

Claims 14, 15, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Ayukawa et al. (US# 6,381,671).

Regarding claim 14, AAPA teaches a semiconductor integrated circuit (100) connected to an external processor (200) Figure 13). Built-in memory (103) stores data as a cache memory for the processor (page 1, lines 21-23). Terminal (104) couples the

processor to the built-in memory. ID-Generation circuit (101) generates production information (ID) about the semiconductor IC (page 1, lines 23-26). The ID is written into the built-in memory when resetting the IC, where the storing upon resetting constitutes that the operation occurs before normal operation has started (page 2, lines 7-12). Although a write circuit as claimed is not explicitly recited, the AAPA recites "storing the ID" in the built-in memory which inherently requires some command circuitry for writing the ID into the built-in memory.

The difference between the claimed subject matter and that of AAPA, disclosed supra, is that the claim recites that the integrated circuit includes a built-in processor. Ayukawa et al. teaches a semiconductor integrated circuit that includes at east a CPU and a memory within a single chip (col. 1, lines 13-31). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Ayukawa et al. at the time the invention was made to modify the memory system of AAPA to include the internal memory with processor like that of Ayukawa et al., because then the number of bus bits could be increased between the CPU and memory in order to enhance data throughput between the memory and CPU logic circuit, as taught by Ayukawa et al.

Regarding claim 15, AAPA teaches that the ID is written into the built-in memory upon an IC system reset, as disclosed above (page 2, lines 7-9).

Regarding claim 18, AAPA teaches that the memory is a cache memory for use by the processor, as disclosed above (page 1, lines 21-23).

Regarding claim 20, AAPA teaches that the production information could include a production history or manufacturer's number (page 1, lines 23-25).

Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Ayukawa et al. (US# 6,381,671), and Ogura (US# 6,181,629).

Regarding claim 16, AAPA teaches storing the ID information when resetting the integrated circuit (page 2, lines 7-9). What AAPA fails to recite is what device causes the (resetting) command to occur. Ogura teaches a semiconductor memory device that includes a (reset) signal under the direction of the CPU (col. 3, lines 61-63). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Ayukawa et al., and Ogura at the time the invention was made to modify the processing system of AAPA and Ayukawa et al. to include the CPU resetting command/signal of Ogura, because then one circuit (CPU) could be responsible for multiple tasks without wasting space on the I.C. with multiple specialized command circuits and thus reduce the manufacturing costs of the I.C.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Ayukawa et al. (US# 6,381,671), and Runaldue et al. (US# 6,178,483).

The difference between the claimed subject matter and that of AAPA, disclosed supra, is that the claims recite a register which receives address data related to the location in the memory to which data is to be stored. Runaldue et al. teaches a register for storing an address for a write operation, where the register receives the address

from a host and stores an address related to the location in the SDRAM memory were the data is to be written (col. 11, lines 15-21). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Ayukawa, and Runaldue et al. at the time the invention was made to modify the memory system of AAPA and Ayukawa et al. to include the address storing register of Runaldue et al., because then a register, a high-speed memory device, could receive and supply the write address to the system in such a way as to reduce processing time, as taught by Runaldue et al.

Allowable Subject Matter

Claims 4, 11, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related system ID procedures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

BRP

5/10/03

Brian Pough
Patent Examiner
Art Unit 2187